AMENDMENTS TO THE CLAIMS:

Claims 1-7, 9, 12-21, 24, 25, and 27-30 were pending at the time of the Office Action.

Claims 1, 3, 7, 9, 13, 16, 19, and 21 are amended.

Claims 1-7, 9, 12-21, 24, 25, and 27-30 remain pending.

1. (Currently amended) A method of performing a numerical simulation, comprising:

programming a programmable device using a plurality of function blocks;

receiving input data;

assigning the received input data to a first portion of the received input data and a second portion of the received input data;

routing ~~a~~ the first portion of the received input data to a processor;

routing ~~a~~ the second portion of the received input data to the programmable device;

performing a first portion of the numerical simulation on the processor using the first portion of the received input data;

performing a second portion of the numerical simulation on the programmable device using the second portion of the received input data;

combining the results of the first and second portions of the numerical simulation; and

outputting the combined results.

2. (Original) The method of Claim 1, further comprising generating a plurality of function blocks.

3. (Currently amended) The method of Claim 2, wherein generating a plurality of function blocks includes generating a plurality of Very High Speed Integrated Circuit Hardware Description Language (VHDL) function blocks.

4. (Previously presented) The method of Claim 1, wherein exchanging data from at least one of the first and second portions via a data path includes providing inputs to a simulation block programmed into the programmable device from the processor via the data path.

5. (Previously presented) The method of Claim 1, wherein exchanging data from at least one of the first and second portions via a data path includes providing outputs from a simulation block programmed into the programmable device to the processor via the data path.

6. (Original) The method of Claim 1, wherein performing a second portion of the numerical simulation on the programmable device includes performing a portion of the original simulation on the programmable device.

7. (Currently amended) The method of Claim 6, wherein performing a portion of the simulation on the programmable device includes:

receiving inputs into a pair of gateway in blocks adapted to ~~deliniate~~ delineate the portions of the simulation to convert into Very High Speed Integrated Circuit Hardware Description Language (VHDL) for operation in hardware.

8. (Cancelled)

9. (Currently amended) The method of Claim 1, wherein performing a portion of a simulation on the programmable device includes:

coupling the outputs of the portion of the simulation to be run in hardware to at least one gateway out block adapted to ~~deliniate~~ delineate the extent of the code to be converted into Very High Speed Integrated Circuit Hardware Description Language (VHDL) for execution in hardware.

10-11 (Cancelled)

12. (Original) The method of Claim 1, further comprising:

forming a synthesis of the function blocks; and

synthesizing a file adapted for use to program gate connections of the programmable device.

13. (Currently amended) A method of performing a numerical simulation, comprising:

generating a plurality of Very High Speed Integrated Circuit Hardware Description Language (VHDL) function blocks;

programming a programmable device using at least some of the plurality of function blocks;

receiving input data;

assigning the received input data to a first portion of the received input data and a second portion of the received input data;

routing ~~a~~ the first portion of the received input data to a processor;

routing ~~a~~ the second portion of the received input data to the programmable device;

performing a first portion of the numerical simulation on the processor using the first portion of the received input data;

performing a second portion of the numerical simulation on the programmable device using the second portion of the received input data;

combining the results of the first and second portions of the numerical simulation; and

outputting the combined results.

14. (Previously presented) The method of Claim 13, wherein exchanging data from at least one of the first and second portions via a data path includes providing inputs to a simulation block programmed into the programmable device from the processor via the data path.

15. (Previously presented) The method of Claim 13, wherein exchanging data from at least one of the first and second portions via a data path includes providing outputs from a simulation block programmed into the programmable device to the processor via the data path.

16. (Currently amended) The method of Claim 13, wherein programming a programmable device includes programming a[[n]] Field Programmable Gate Array (FPGA) device using at least some Very High Speed Integrated Circuit Hardware Description Language (VHDL) function blocks, and wherein performing a second portion of the numerical simulation on the programmable device includes performing a[[n]] Fast Fourier Transform (FFT) on the programmable device.

17. (Original) The method of Claim 16, wherein performing a portion of a simulation on the programmable device includes:

receiving inputs via the data path into a pair of gateway in blocks;

coupling the output of the double delay block to a third input of the FFT block, the third input being adapted to mark data input as valid or invalid;

coupling the output of a k=0 block to a fourth input of the FFT block, the fourth input being adapted to control a forward or a reverse transform;

providing a real component output from the FFT block;

providing an imaginary component output from the FFT block;

providing a third output from the FFT block adapted to mark the output data as valid or invalid;

providing a fourth output from the FFT block that is active high on a first output sample in a frame;

providing a fifth output from the FFT block that is active high when the FFT block can accept data;

coupling the real component output, imaginary component output, third output, fourth output, and fifth output from the FFT block to at least one D flip flop-based registers adapted to provide a signal latency; and

coupling the outputs of the registers to at least one gateway out.

18. (Original) The method of Claim 13, further comprising:

forming a synthesis of the function blocks; and

synthesizing a file adapted for use to program gate connections of the programmable device.

19. (Currently amended) An apparatus for performing a numerical simulation, comprising:

an input device configured ~~adapted~~ to receive input data including a real input and an imaginary input;

a processor;

a programmable device; and

a module,

wherein:

the module ~~routs~~ routes a first portion of the received input data to the processor and ~~routs~~ routes a second portion of the received input data to the programmable device;

the processor is configured ~~adapted~~ to perform a first portion of the numerical simulation using the first portion of the received input data;

the programmable device is configured ~~adapted~~ to use at least some function blocks to perform a second portion of the numerical simulation, using the second portion of the received input data; and

the module is configured to ~~combines~~ the results of the first and second portions of the numerical simulation.

20. (Original) The apparatus of Claim 19, further comprising a generator adapted to generate a plurality of function blocks, at least some of the function blocks being adapted to perform a respective part of the second portion of the numerical simulation.

21. (Currently amended) The apparatus of Claim 20, wherein the generator is further adapted to generate a plurality of Very High Speed Integrated Circuit Hardware Description Language (VHDL) function blocks.

22-23 (Cancelled)

24. (Original) The apparatus of Claim 19, the programmable device is further adapted to perform a simulation function block.

25. (Original) The apparatus of Claim 24, wherein the programmable device is further adapted to:

receive inputs into a pair of gateway in.

26. (Cancelled)

27. (Previously presented) The method of Claim 1, wherein routing a second portion of the received input data to the programmable device comprises selecting the most time consuming portion of the numerical simulation to be routed to the programmable device.

28. (Previously presented) The method of Claim 27, wherein selecting the most time consuming portion of the numerical simulation comprises selecting a portion of the numerical simulation that includes at least one logical operation.

29. (Previously presented) The apparatus of Claim 19, wherein routing a second portion of the received input data to the programmable device comprises selecting the most time consuming portion of the numerical simulation to be routed to the programmable device.

30. (Previously presented) The apparatus of Claim 29, wherein selecting the most time consuming portion of the numerical simulation comprises selecting a portion of the numerical simulation that includes at least one logical operation.